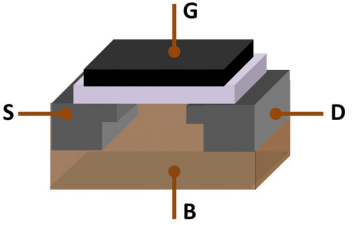
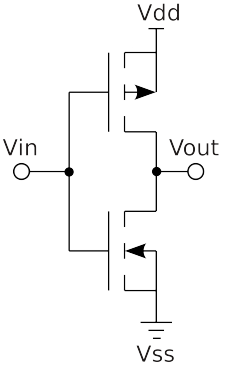
Discussion 1B

Transistors

Logo credits go to Moses Won





About Me

(Super) Senior CS & Math Double Major
4th time TAing this class, taught 16A for a year

Academic Interests: Machine Learning, Control Theory, Probability

Hobbies: Soccer, Basketball, Classical Music, Board Games

Personal Website: taejin.xyz/teaching

Will upload recordings, notes, and occasional practice problems.

Discussion 1B: Transistors

What is a transistor?

Transistors are electrical devices that **switch** or **amplify** electrical signals and power.

Common Terminology

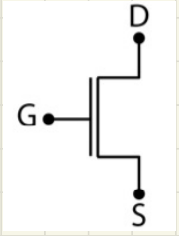
MOS: Metal-Oxide Semiconductor
FET: Field-Effect Transistor

BJT: Bipolar Junction Transistor

CMOS Transistors

C stands for “Complementary”

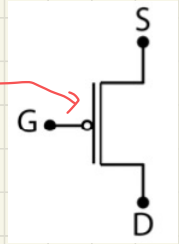
NMOS



NMOS:
Drain: Higher
Source: Lower

N stands for N-Type

PMOS



Notice the bubble in the PMOS

PMOS:
Source: Higher
Drain: Lower

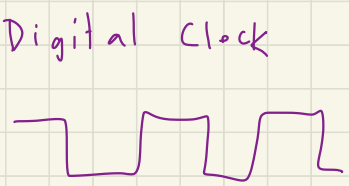
P stands for P-Type

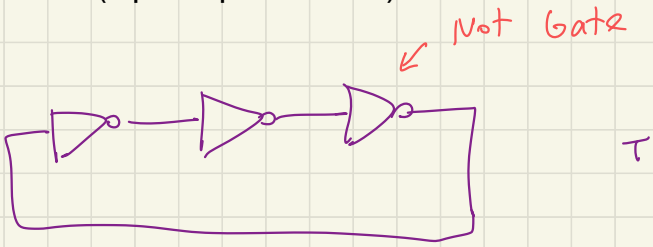
"Type" refers to the semiconductor material that makes these transistors. (Out of scope)

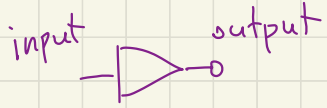
Why do we care about transistors?

Some call it the greatest invention of the 20th century!

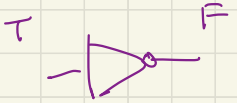
- We can build logic gates out of CMOS Transistors
- You can build a CPU with logic gates and a clock (61C Logisim Project)
- A clock can be made out of transistors. (Ring oscillator)
- We can amplify signals using transistors. (Op-Amps are a lie)







Input.	out.
T	F
F	T



takes some time to switch from T → F

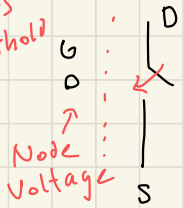
Breakdown of a Transistor

NMOS

V_{tn}: NMOS Threshold

$V_{GS} = V_G - V_S$

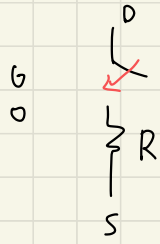
Switch Model



Node Voltage

Closed when $V_{GS} \geq V_{tn}$

Resistor - Switch Model

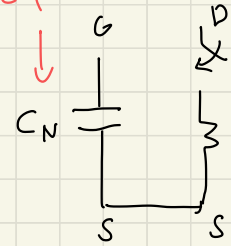


Closed when $V_{GS} \geq V_{tn}$

↑ Internal Resistance

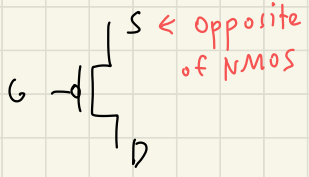
Parasitic Capacitance

RC Model



Closed when $V_{GS} \geq V$

PMOS

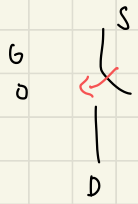


S ← opposite of NMOS

$V_{SG} = V_S - V_G$

V_{tp}: PMOS threshold

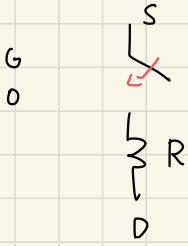
Switch Model



$V_{SG} \geq |V_{tp}|$

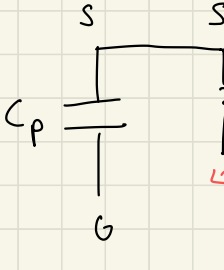
PMOS has a negative threshold potential

Resistor - Switch Model



$V_{SG} \geq |V_{tp}|$

RC Model



$V_{SG} \geq |V_{tp}|$

Uses

Switch Model

Analyze Logical behavior of transistor

Resistor-Switch

Analyze Power Consumption

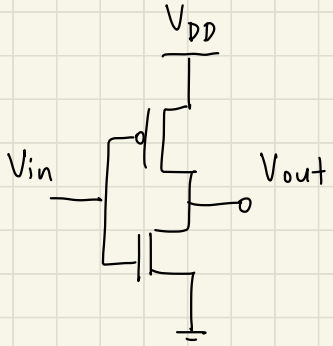
RC Model

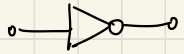
Analyze the time delay of each transistor

Normally PMOS is ON when $V_{GS} \leq V_{tp}$

$V_{SG} \geq |V_{tp}|$

CMOS Inverter



The CMOS Inverter is a NOT Gate 

We define 0V as a logical False and $V_{DD} = 5V$ as a logical True. Suppose $V_{tn} = |V_{tp}| = \frac{V_{DD}}{2}$

Expected

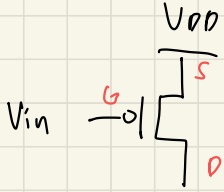
Vin	Vout
T	F
F	T

In Circuits

Vin	Vout
V_{DD}	
0V	

$V_{out} = 0V$

Assume V_{in} = True = V_{DD}



$V_G = V_{in} = V_{DD}$

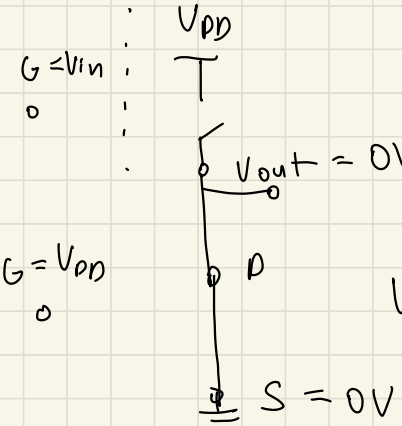
$V_S = V_{DD}$ $V_D = V_{out}$

$V_{SG} = V_S - V_G$
$= V_{DD} - V_{DD}$
$= 0$

Ask: Is $0 \geq |V_{tp}|$?

No: switch is off / open

New Circuit (Assume switch model)

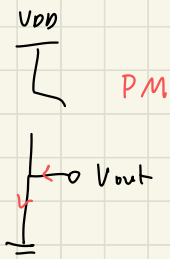


$V_{GS} = V_{DD} > V_{tn} =$

Ex: $V_{tn} > V_{DD}$

$V_{in} = V_{DD}$ or $V_{in} = T$

Circuit

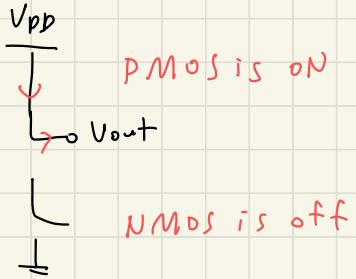


Vout is connected to ground so

$V_{out} = 0V$

$V_{in} = 0$ or $V_{in} = F$

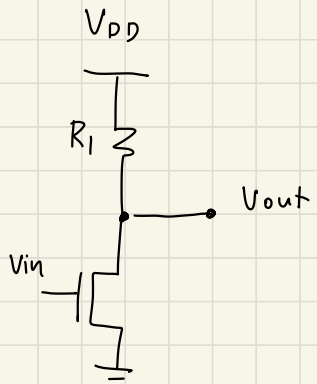
Circuit



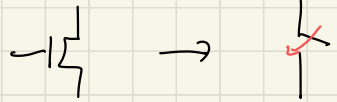
Vout is connected to V_{DD} so

$V_{out} = V_{DD}$

3. Single Transistor Inverter



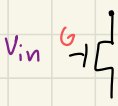
Switch Model



$V_{GS} \geq V_{th}$ $\quad 0 < V_{th} < V_{DD}$

(i) What is V_{out} when $V_{in} = 0V$

1. Label G, D, S
2. Calculate V_{GS}
3. Switch is on/off?

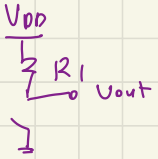


$V_G = V_{in}$, $V_S = 0$, $V_D = V_{out}$

$V_{GS} = V_G - V_S$
$= V_{in} - 0$
$= 0$

$V_{GS} = 0 < V_{th}$
So switch is off/open

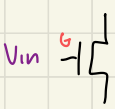
4. Resulting Circuit:



$V_{out} = V_{DD}$ since $i_{R1} = 0$

(ii) What is V_{out} when $V_{in} = V_{DD}$?

1. Label G, D, S
2. Calculate V_{GS}
3. Switch on/off?

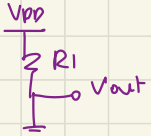


$V_G = V_{DD}$, $V_S = 0$, $V_D = V_{out}$

$V_{GS} = V_G - V_S$
$= V_{DD} - 0$
$= V_{DD}$

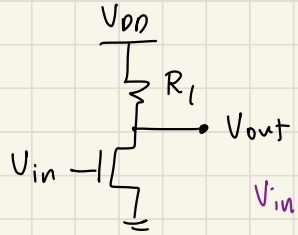
$V_{GS} = V_{DD} > V_{th}$
So switch is on/closed

4. Resulting Circuit:

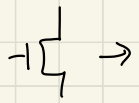


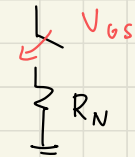
$V_{out} = 0$ since V_{out} is connected to ground.

Part 2: Using resistor-switch model



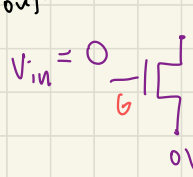
Not Gate





$0 < V_{tn} < V_{DD}$

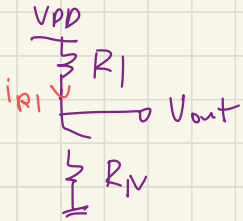
(i) What is V_{out} when $V_{in} = 0$?



$V_{GS} = V_G - V_S$

$= 0 - 0 = 0 < V_{tn}$

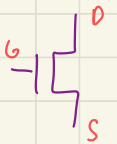
NMOS is off / open



$i_{R_1} = 0$ since nothing is connected

$V_{out} = V_{DD}$

(ii) What is V_{out} when $V_{in} = V_{DD}$?



$G = V_{in} = V_{DD}$

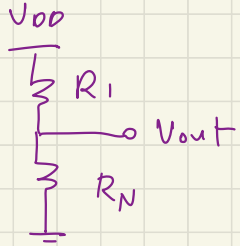
$S = 0V$

$D = V_{out}$

$V_{GS} = V_{DD} > V_{tn}$

NMOS is on / closed

$R_N = \frac{1}{10} R_1$



Voltage Dividers: $V_{out} = \frac{R_N}{R_1 + R_N} V_{DD} = \frac{1}{11} V_{DD}$

↑ Doesn't reach true 0.

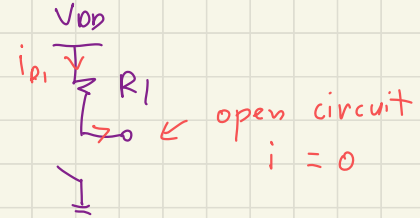
Using this inverter, designers should label $\frac{1}{11} V_{DD}$ as False or create some threshold H if $V < H$, then V is False

Here $H \approx \frac{1}{10} V_{DD}$ will suffice.

(iii) How much power does this circuit consume when $V_{in} = 0$?

Remember $P = IV$.

When $V_{in} = 0V$



Since $i = 0$, $P = 0$.

(iv) How much power does this circuit consume when $V_{in} = V_{DD}$?

$$i = \frac{V_{DD}}{R_1 + R_N}$$

$V = V_{DD}$ since power is consumed across both resistors.

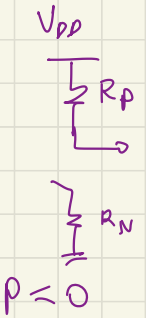
$$P = \frac{V_{DD}^2}{R_1 + R_N}$$

(v) Compare to CMOS Inverter:

CMOS inverter consumes zero power

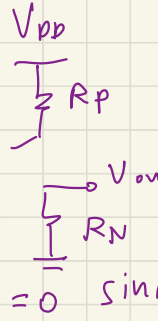
This is why CMOS is desirable over single NMOS transistor.

$V_{in} = 0V$



$P = 0$

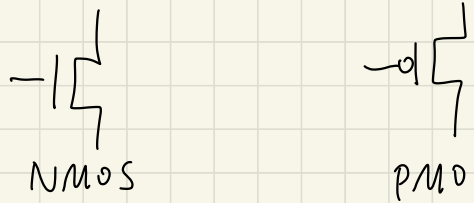
$V_{in} = V_{DD}$



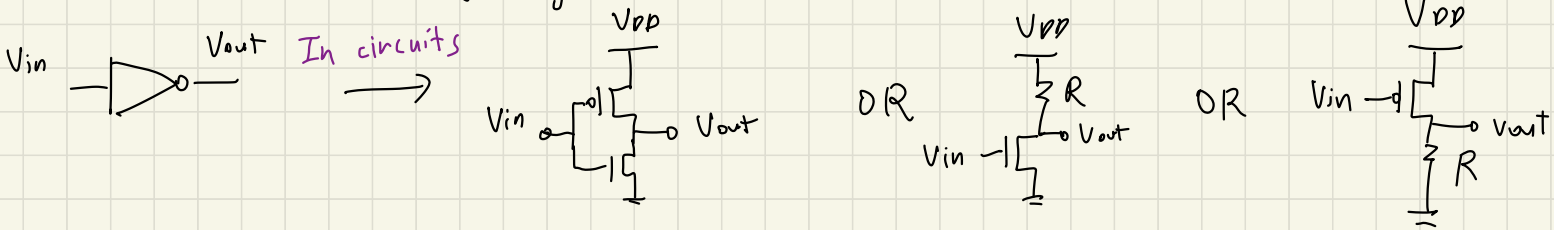
$P = 0$ since $V_{out} = 0$

Summary (Main Takeaways)

1. Two Transistors (PMOS and NMOS), they behave like switches



2. We can build Logic gates out of Transistors



3. CMOS Inverter is desirable over single NMOS / PMOS since CMOS consumes zero power when no load is attached.

4. Looking Forward: Transistors always have delay due to parasitic capacitance.