1 Transistor Introduction

Transistors (as presented in this course) are 3 terminal, voltage controlled switches. This means that, when a transistor is "on," it connects the Source (S) and Drain (D) terminals via a low resistance path (short circuit). When a transistor is "off," the Source and Drain terminals are disconnected (open circuit).

Two common types of transistors are NMOS and PMOS transistors. Their states (shorted or open) are determined by the voltage difference across the Gate (G) and Source (S) terminals, compared to a "threshold voltage." Transistors are extremely useful in digital logic design since we can implement Boolean logic operators using switches.

Recall that in this class, V_{tn} denotes how much **higher** the gate needs to be relative to the source for the NMOS to be on, and that $|V_{tp}|$ denotes how much **lower** the gate needs to be relative to the source for the PMOS to be on.

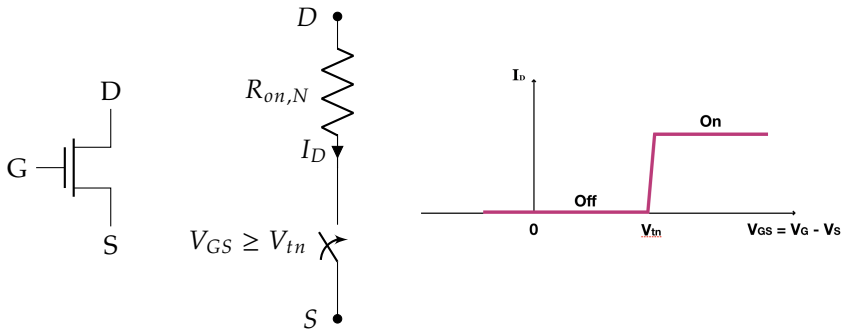


Figure 1: NMOS Transistor Resistor-switch model

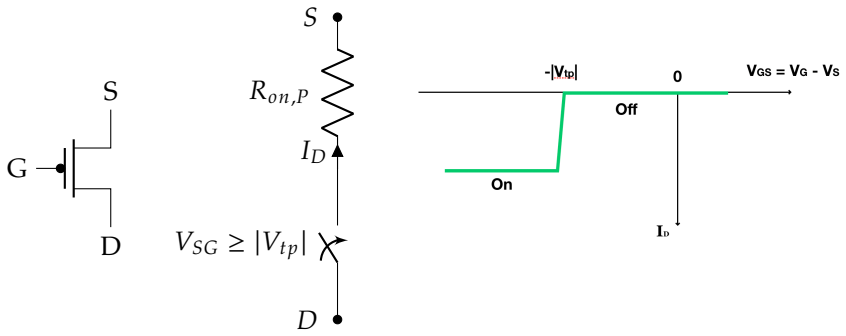


Figure 2: PMOS Transistor Resistor-switch model

Transistors can be connected together to perform boolean algebra. For example, the following circuit is called an "inverter" and represents a NOT

gate.

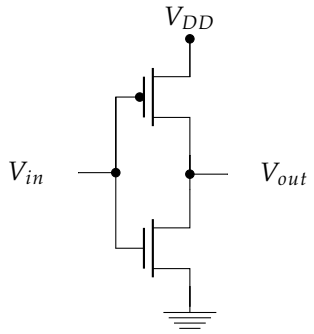


Figure 3: CMOS Inverter

When the input is high ($V_{in} \geq V_{tn}$, $V_{in} \geq V_{DD} - |V_{tp}|$), then the NMOS transistor is on, the PMOS transistor is off, and $V_{out} = 0$. When the input is low ($V_{in} \leq V_{tn}$, $V_{in} \leq V_{DD} - |V_{tp}|$), the NMOS transistor is off, the PMOS transistor is on, and $V_{out} = V_{DD}$. When working with digital circuits like the one above, we usually only consider the values of $V_{in} = 0, V_{DD}$. This yields the following truth table:

V_{in}	V_{out}	NMOS	PMOS
V_{DD}	0	on	off
0	V_{DD}	off	on

If you think of V_{DD} being a logical 1 and 0 V being a logical 0, we have just created the most elementary logical operation using transistors!

2 KVL/KCL Review

Use Kirchhoff's Laws on the circuit below to find V_x in terms of V_{in}, R_1, R_2, R_3.

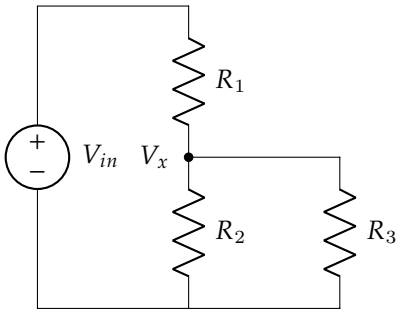


Figure 4: Example Circuit

a) What is V_x?

Answer

Applying KCL to the node at V_x, we get

$$\frac{V_x - V_{in}}{R_1} + \frac{V_x}{R_2} + \frac{V_x}{R_3} = 0$$

Solving this equation for V_x yields

$$V_x = V_{in} \frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

b) As $R_3 \to \infty$, what is V_x? What is the name we used for this type of circuit?

Answer

As $R_3 \to \infty$, the $R_1 R_2$ term on the denominator will become insignificant, simplifying our expression.

$$\begin{aligned}
\lim_{R_3 \to \infty} V_x &= \lim_{R_3 \to \infty} V \frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3} \\
&= V_{in} \lim_{R_3 \to \infty} \frac{R_2 R_3}{R_1 R_3 + R_2 R_3} \\
&= V_{in} \lim_{R_3 \to \infty} \frac{(R_2) R_3}{(R_1 + R_2) R_3} \\
&= V_{in} \frac{R_2}{R_1 + R_2}
\end{aligned}$$

When $R_3 \to \infty$, it effectively becomes an open wire, which makes the rest of the circuit a voltage divider, or resistive divider.

3 Single-transistor Inverter

Consider the following single-transitor inverter, consisting of an NMOS transistor and a resistor, where for N_1 we have $0 < V_{tn} < V_{DD}$.

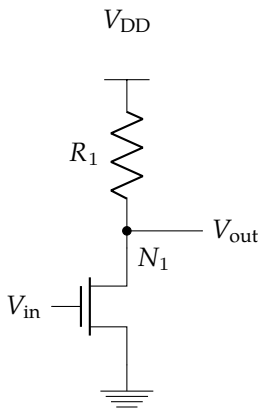


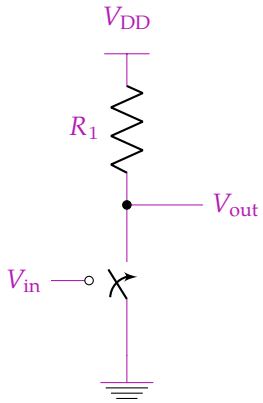
Figure 5: Single transistor NMOS inverter

a) Replace the transistor N_1 with a switch, the simplest model of a transistor and answer the following questions

   a) What is V_{out} when $V_{in} = 0$?

Answer

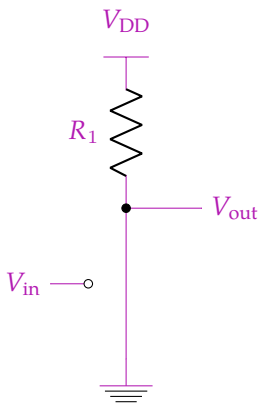
When $V_{in} = 0$ the transistor lets no current through (the switch is open) and $V_{out} = V_{DD}$



   b) What is V_{out} when $V_{in} = V_{DD}$?

Answer

When $V_{in} = V_{DD}$ the transistor lets current through (the switch is closed) and $V_{out} = 0$



c) What is the power consumption of the circuit when $V_{in} = 0$? How about when $V_{in} = V_{DD}$

Answer

Recall that $P = IV$. If $V_{in} = 0$, $I = 0$ and there is no power.

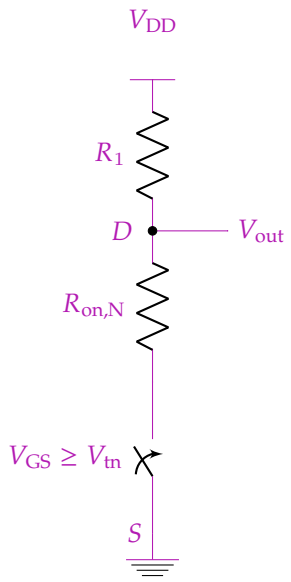
However, if $V_{in} = V_{DD}$, the power disipated by the resistor is $P = IV = \frac{V_{DD}^2}{R_1}$

b) Now replace the NMOS device with a transistor model that includes an internal resistor, such as the one in Figure 1

a) What is V_{out} when $V_{in} = 0$?

Answer

In this case, the circuit looks as below, with the switch open. Since no current flows, $V_{out} = V_{DD}$.



b) What is V_{out} when $V_{in} = V_D D$ in terms of R_1 and $R_{on,N}$?
What is this value if $R_{on,N} = \frac{1}{10} R_1$?
How much power does the circuit consume?

Answer

The circuit in question is the one above, with the switch closed. This is a voltage divider with $V_{out} = \frac{R_{on,N}}{R_{on,N} + R_1} V_{DD}$. With the value for $R_{on,N}$, we have $V_{out} = \frac{1}{11} V_{DD}$. Note that this value may be close to 0, but now we cannot reach a true "low" output state.

The power is

$$P = IV = \frac{V_{DD}^2}{(R_{on,N} + R_1)}.$$

c) Now consider a CMOS inverter with both PMOS and CMOS devices, such as that of Figure 4. How does the performance and power consumption compare?

Answer

Note that for the CMOS inverter, there is always at least one switch that is open and does not let current through, leading to essentially zero power consumption (in reality there is always some power consumption, and this analysis assumes no load at the output) in both states. On the other hand,

the inverter presented in this problem consumes power when $V_{\text{in}} = V_{\text{DD}}$. Moreover, the inverter presented in this problem does not reach "both rails"(ground and V_{DD}) since the transistor has some resistance when it is on.

4 NAND Circuit

Let us consider a NAND logic gate. This circuit implements the boolean function $\overline{(A \cdot B)}$.

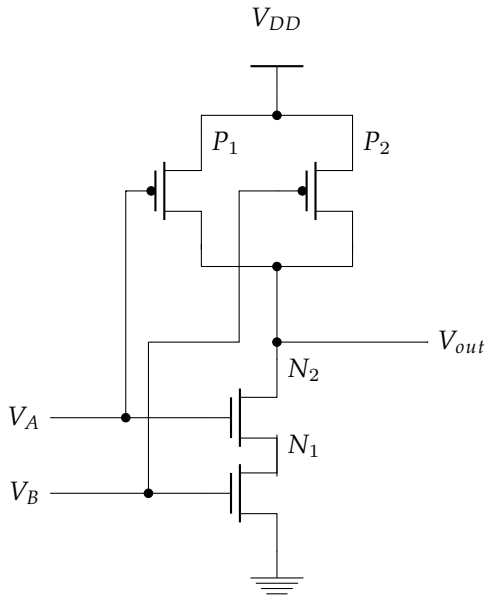


Figure 6: NAND

V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

Answer

In an NMOS, the terminal at the higher potential is always the drain, and the terminal at the lower potential is always the source. Therefore, the drain is at the top of N_2 (connected to V_{out}) and the top of N_1 (connected to N_2). The source is at the bottom of N_2 (connected to N_1) and the bottom of N_1 (connected to ground). The gate terminal of N_2 is connected to V_A; the gate of N_1 is connected to V_B. In an PMOS, the terminal at

the higher potential is always the source, and the terminal at the lower potential is always the drain. Therefore, the source is at the top of P_1 and P_2 (connected to V_{DD}). The drain is at the bottom of P_1 and P_2 (connected to V_{out}). The gate terminal of P_1 is connected to V_A; the gate of P_2 is connected to V_B.

b) If $V_A = V_{DD}$ and $V_B = V_{DD}$, which transistors act like open circuits? Which transistors act like closed circuits? What is V_{out}?

Answer

P_1 and P_2 are off, creating an open circuit. N_1 and N_2 are on, creating a closed circuit. $V_{out} = 0V$ because it is connected by closed circuit to ground.

c) If $V_A = 0V$ and $V_B = V_{DD}$, what is V_{out}?

Answer

P_2 and N_2 are off, creating an open circuit. P_1 and N_1 are on, creating a closed circuit. $V_{out} = V_{DD}$ because it is connected by closed circuit to V_{DD}.

d) If $V_A = V_{DD}$ and $V_B = 0V$, what is V_{out}?

Answer

P_1 and N_1 are off, creating an open circuit. P_2 is on, creating a closed circuit. $V_{out} = V_{DD}$ because it is connected by closed circuit to V_{DD}.

Note that with the simplest transistor model, one cannot to determine V_{GS} for N_2, since we don't know the source voltage for that transistor. V_{out} is still high, because regardless of whether N_2 is on, there is an open (or very high resistance) between V_{out} and ground while there is a short to V_{DD}.

e) If $V_A = 0V$ and $V_B = 0V$, what is V_{out}?

Answer

N_1 is off, creating an open circuit. P_1 and P_2 are on, creating a closed circuit. $V_{out} = V_{DD}$ because it is connected by closed circuit to V_{DD}.

Like above, the source of N_1 has an ambigous value and we cannot determine whether N_1 is on or off. However, this does not affect the output because the path to ground is an open since N_1 is off.